CLAIMS

1. A transistor device having a metallic source electrode, a metallic drain electrode, a metallic gate electrode and a channel in a deposited semiconductor material, the transistor device comprising:
a first layer comprising the metallic gate electrode, a first metal portion of the metallic source electrode and a first metal portion of the metallic drain electrode;
a second layer comprising a second metal portion of the metallic source electrode, a second metal portion of the metallic drain electrode, the deposited semiconductor material and dielectric material between the semiconductor material and the metallic gate electrode; and
a third layer comprising a substrate, wherein the first, second and third layers are arranged in order such that the second layer is positioned between the first layer and the third layer.

2. A transistor device as claimed in claim 1, wherein the metallic source electrode, drain electrode and gate electrode comprise electro-deposited metal.

3. A transistor device as claimed in claim 1 or 2, wherein the first, second and third layers are each of respective substantially uniform thickness.

4. A transistor device as claimed in claim 1, 2 or 3, wherein the third layer includes adhesive bonding the passive substrate to the transistor device.

5. A transistor device as claimed in any one of claims 1 to 4, wherein the first layer has a substantially planar surface comprising substantially planar portions of the source, drain and gate electrodes.

6. A transistor device as claimed in any one of claims 1 to 5, wherein the deposited semiconductor material comprises organic semiconductor material.

7. A transistor device as claimed in any one of claims 1 to 6, wherein the deposited semiconductor material comprises indications that it was deposited from liquid.

8. A transistor device as claimed in any one of claims 1 to 7, wherein the semiconductor material is embedded in the device and overlain by the gate electrode.

9. A transistor device as claimed in any preceding claim wherein the first layer comprises insulating material separating the gate electrode from the source electrode and the drain electrode.

10. A transistor device as claimed in claim 9, wherein the insulating material is photo-patternable.

11. A transistor device as claimed in any preceding claim wherein the substrate is flexible.

12. A substrate for a display device comprising a plurality of transistor devices as claimed in any preceding claim.

13. A method for use in forming a transistor device comprising:
(i) forming a transfer layer on a conductive carrier;
(ii) fixing the transfer layer to a substrate; and
(iii) removing the conductive carrier, wherein the transfer layer is formed in step (i) by:

a) selectively masking the conductive carrier, to expose first, second and third portions of the conductive carrier;

b) electro-depositing metal onto the first, second and third portions of the conductive carrier to form first, second and third metal portions;

c) depositing dielectric material over at least the second metal portion;

d) electro depositing metal on the first and third metal portions; and

e) depositing semiconductor material over the dielectric layer.

14. A method as claimed in claim 13, wherein the step of selectively masking the conductive carrier includes the selective formation of insulating material on portions of the conductive carrier and the retention of the insulating material within the transistor device.

15. A method as claimed in claim 13 or 14, wherein the transfer layer provides a terminal layer of the device.

16. A method as claimed in claim 13, 14 or 15, wherein the step of fixing the transfer layer to a substrate portion embeds semiconductor material within the device.

17. A method as claimed in any one of claims 13 to 16, wherein the semiconductor material deposited in step e) is selectively deposited between the metal deposited in step d).

18. A method as claimed in any one of claims 13 to 16, wherein the step e) precedes step d).

19. A method as claimed in any one of claims 17 to 20, further comprising the step of passivating the conductive carrier before step a).

20. A method as claimed in any one of claims 13 to 19, wherein the conductive carrier is of substantially uniform thickness.

21. A method as claimed in any one of claims 13 to 20, wherein the step of fixing the transfer layer to the substrate involves the application of a curable adhesive to the substrate, the contacting of the adhesive layer and the transfer layer and the curing of the adhesive.

22. A semiconductor device formed using the method as claimed in any one of claims 13 to 21.

23. A device or method substantially as hereinbefore described with reference to and/or as shown in the accompanying drawings.

24. Any novel subject matter or combination including novel subject matter disclosed, whether or not within the scope of or relating to the same invention as the preceding claims.

25. A transistor device having a metallic source electrode, a metallic drain electrode, a metallic gate electrode and a channel in a deposited semiconductor material, the transistor device comprising:

a first upper planar layer comprising the metallic gate electrode, a first metal portion of the metallic source electrode and a first metal portion of the metallic drain electrode;

a second middle planar layer comprising a second metal portion of the metallic source electrode, a second metal portion of the metallic drain electrode, the deposited semiconductor material and dielectric material between the semiconductor material and the metallic gate electrode; and

a third lower planar layer comprising a substrate, wherein first, second and third planar layers are arranged in order such that the second middle layer is positioned between the first upper layer and the third lower layer,

wherein the metallic source electrode, drain electrode and gate electrode comprise electro-deposited metal, the gate electrode occupies only the first upper planar layer and the channel occupies only the second middle planar layer, the metallic source electrode consists of the first metal portion of the metallic source electrode overlying the second metal portion of the metallic source electrode and the metallic drain electrode consists of the first metal portion of the metallic drain electrode overlying the second metal portion of the metallic drain electrode

26. A transistor device as claimed in any one of claims 1 to 12 or claim 25, wherein the metallic source, gate and drain electrodes consist entirely of electro-deposited material and the metallic gate electrode contacts the dielectric material.